AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method for performing a timing analysis for a core device to be embedded in a programmable logic, comprising:

obtaining clock-to-output timing information for the core device;

determining setup and hold timing information and delay timing information for a portion of the programmable logic device;

associating the clock-to-output timing information, the setup and hold timing information and the delay timing information with respective signals; and

calculating a path time delay for each of the respective signals.

2. (Original) The method of Claim 1 further comprising determining whether the path time delay for each of the respective signals is less than a clock period.

3. (Original) The method of Claim 2 further comprising modifying the portion of the host integrated circuit in response to the path time delay for at least one of the respective signals being more than the clock period.

4. (Previously Presented) The method of Claim 3 further comprising determining circuitry values in response to modification of the portion of the programmable logic device.

5. (Previously Presented) The method of Claim 3 further comprising feeding back the circuitry values and modifications of the portion of the programmable logic device for re-determination of at least one of the setup and hold timing information and the delay timing information for the portion of the programmable logic device.

6. (Previously Presented) The method of Claim 5 wherein the portion of the programmable logic device comprises logic and interconnects for coupling the core device to the programmable logic device.

7. (Previously Presented) The method of Claim 6 wherein the portion of the programmable logic device comprises a memory controller coupled to the logic and interconnects.

8. (Previously Presented) The method of Claim 7 wherein the core device is a microprocessor.

9. (Original) The method of Claim 8 wherein the programmable logic device is a field programmable gate array.

10. (Previously Presented) A method for performing a timing analysis for [[an]] a core device in a host integrated circuit, comprising:

obtaining setup and hold timing information for the core device;

determining clock-to-output timing information and delay timing information for a portion of the host integrated circuit;

associating the clock-to-output timing information, the setup and hold timing information and the delay timing information with respective signals; [[and]]

calculating a path time delay for each of the respective signals; and

feeding back circuitry values and modifications of the portion of the host integrated circuit for re-determination of at least one of the clock-to-output timing information and the delay timing information for the portion of the host integrated circuit.

11. (Original) The method of Claim 10 further comprising determining whether the path time delay for each of the respective signals is less than a clock period.

12. (Original) The method of Claim 11 further comprising modifying the portion of the host integrated circuit is in response to the path time delay for at least one of the respective signals being more than the clock period.

13. (Original) The method of Claim 12 further comprising determining circuitry values in response to modification of the portion of the host integrated circuit.

14. (Cancelled)

15. (Previously Presented) The method of Claim 12 wherein the portion of the host integrated circuit comprises logic and interconnects for coupling the core device to the host integrated circuit.

16. (Original) The method of Claim 15 wherein the portion of the host integrated circuit comprises a memory controller coupled to the logic and interconnects.

17. (Original) The method of Claim 16 wherein the core device is a microprocessor, and wherein the host integrated circuit is a programmable logic device.

18. (Original) The method of Claim 17 wherein the programmable logic device is a field programmable gate array.

19. (Withdrawn) A method for determining timing performance, comprising:

obtaining clock-to-output times for a processor core;

using static timing analysis to determine timing data for a memory controller;

obtaining setup and hold times from the timing data for the memory controller;

providing a programmatic representation of logic and interconnects for coupling the memory controller and the processor core;

simulating the programmatic representation of logic and interconnects to obtain delay times;

inputting the delay times, the setup and hold times and the clock-to-output times to a spreadsheet; and

determining path times from the spreadsheet.

20. (Withdrawn) The method of Claim 19 further comprising comparing timing of at least one of the path times to a clock period.

21. (Withdrawn) The method of Claim 20 wherein the clock-to-output times are expressed in a Standard Delay Format.

22. (Withdrawn) The method of Claim 19 wherein the step of inputting comprises associating a delay time of the delay times, a setup and hold time of the setup and hold times, and a clock-to-output time of the clock-to-output times to an output signal from the processor core.

23. (Withdrawn) The method of Claim 22 wherein the delay time, the setup and hold time and the clock-to-output time are totaled in the step of determining to provide a path time.

24. (Withdrawn) The method of Claim 23 further comprising comparing the path time to a clock period.

25. (Withdrawn) The method of Claim 24 wherein the memory controller and the processor core are to be part of a programmable logic device, wherein the processor core is to be embedded in the programmable logic device.

26. (Withdrawn) The method of Claim 25 wherein the memory controller and the processor core are laid out according to different lithographic minimum dimensions.

27. (Withdrawn) A method for determining timing performance, comprising:

obtaining setup and hold times for a processor core;

using static timing analysis to determine timing data for a memory controller;

obtaining clock-to-output times from the timing data for the memory controller;

providing a programmatic representation of logic and interconnects for coupling the memory controller and the processor core;

simulating the programmatic representation of logic and interconnects to obtain delay times;

inputting the delay times, the setup and hold times and the clock-to-output times to a spreadsheet; and

determining path times from the spreadsheet.

28. (Withdrawn) The method of Claim 27 further comprising comparing timing of at least one of the path times to a clock period.

29. (Withdrawn) The method of Claim 28 wherein the clock-to-output times are expressed in a Standard Delay Format.

30. (Withdrawn) The method of Claim 27 wherein the step of inputting comprises associating a delay time of the delay times, a setup and hold time of the setup and hold times, and a clock-to-output time of the clock-to-output times to an output signal from the processor core.

31. (Withdrawn) The method of Claim 30 wherein the delay time, the setup and hold time and the clock-to-output time are totaled in the step of determining to provide a path time.

32. (Withdrawn) The method of Claim 31 further comprising comparing the path time to a clock period.

33. (Withdrawn) The method of Claim 32 wherein the memory controller and the processor core are to be part of a programmable logic device, wherein the processor core is to be embedded in the programmable logic device.

34. (Withdrawn) The method of Claim 33 wherein the memory controller and the processor core are laid out according to different lithographic minimum dimensions.